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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LE, LANA N	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,388	DIJKMANS ET AL.	
	Examiner	Art Unit	
	Lana N. Le	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 3/09/06

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 3-9,11-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 3-9,11-21 is/are rejected.

7)☒ Claim(s) 22-23 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vishakhadatta et al (US 2002/0,141,511) in view of Maligeorgos (US 2002/0,039,039).

Regarding claim 3, Vishakhadatta et al disclose a high frequency receiver (839, 851), which front end comprises a low noise amplifier (LNA circuitry 824), which is provided with a front end comprising a low noise amplifier (LNA circuitry 824), and which is provided with quadrature mixers (dowconverting circuitry comprising I and Q mixers producing I and Q outputs) coupled to the low noise amplifier (2), characterized in that the low noise amplifier is a quadrature low noise amplifier (LNA circuitry with in phase and quadrature outputs; para. 79; fig. 8). Vishakhadatta et al fail to further disclose the receiver is characterized in that quadrature paths of the quadrature low noise amplifier are implemented differentially. Maligeorgos discloses receiver is characterized in that quadrature paths (I and Q outputs) of the quadrature amplifier (24, 26) are implemented differentially (para. 30). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to implement differentially the amplifiers of Vishakhadatta et al in order to distinguish the two separate in phase and quadrature characteristics of the amplifier by suppressing outputs from common mode interference on its input.

Regarding claim 11, Vishakhadatta et al disclose a quadrature low noise amplifier (LNA circuitry with in phase and quadrature outputs; para. 79; fig. 8) for application in the high frequency receiver (high RF frequency in i.e. PCS, GSM, DCS bands; 839, 851) of Vishakhadatta et al and Maligeorgos according to claim 3.

Regarding claim 12, Vishakhadatta et al disclose a method for receiving high frequency signals, comprising:

implementing quadrature low noise amplifier (LNA circuitry with in phase and quadrature outputs; para. 79; fig. 8), disposed at a front end of a high frequency receiver; and coupling quadrature mixers (dowconverting circuitry comprising I and Q mixers producing I and Q outputs) to the amplifier (2). Vishakhadatta et al fail to further disclose the method is characterized in that quadrature paths of the quadrature low noise amplifier are implemented differentially. Maligeorgos discloses a receiver characterized in that quadrature paths (I and Q outputs) of a quadrature amplifier (24, 26) are implemented differentially (para. 30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differentially the amplifiers of Vishakhadatta et al in order to distinguish the two separate in phase and quadrature characteristics of the amplifier.

Regarding claim 16, Vishakhadatta et al and Maligeorgos disclose the method of claim 12, wherein Vishakhadatta et al disclose the coupled quadrature mixers (dowconverting circuitry comprising I and Q mixers producing I and Q outputs) are in a receive circuit of said receiver (fig. 8).

Regarding claim 17, Vishakhadatta et al and Maligeorgos disclose the method of claim 16, wherein Vishakhadatta et al disclose the output of said mixer (409) comprises a signal (412, 415) that has been downconverted by said receive circuit.

Regarding claim 18, Vishakhadatta et al and Maligeorgos disclose the receiver of claim 3, wherein Vishakhadatta et al disclose the coupled quadrature mixers (409) are in a receive circuit of said receiver (fig. 8).

Regarding claim 19, Vishakhadatta et al and Maligeorgos disclose the receiver of claim 18, wherein Vishakhadatta et al disclose output of said mixers (409) comprises a signal (412, 415) that has been down-converted by said receive circuit of fig. 8.

3. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vishakhadatta et al (US 2002/0,141,511) in view of Maligeorgos (US 2002/0,039,039). and further in view of Franca-Neto (US 6,509,799).

Regarding claim 20, Vishakhadatta et al and Maligeorgos disclose the receiver of claim 7, wherein Vishakhadatta et al, Maligeorgos do not disclose the cascode arrangement comprises two parallel legs of said semiconductors, both legs being in parallel with said capacitor. Franca-Neto disclose the cascode arrangement comprises two parallel legs of said semiconductors, both legs being in parallel with said capacitor (fig. 3, lines 7-41). It would have been obvious to one of ordinary skill in the art at the

time the invention was made to have the cascode arrangement comprise two parallel semiconductors in parallel with the capacitor in order to implement the cascade arrangement differentially to

Regarding claim 21, Vishakhadatta et al and Maligeorgos disclose the receiver of claim 7, wherein Vishakhadatta et al and Maligeorgos fail to disclose said cascode arrangement comprises differential cascade arrangement. Franca-Neto disclose a cascode arrangement comprises differential cascade arrangement (fig. 2; col 4, lines 14-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to distinguish the two separate in phase and quadrature characteristics of the amplifier by suppressing outputs from common mode interference on its input.

4. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vishakhadatta et al (US 2002/0,141,511) in view of Maligeorgos (US 2002/0,039,039). and further in view of Sano et al (US 5,546,048).

Regarding claim 4, Vishakhadatta et al and Maligeorgos disclose the method of claim 3, wherein Vishakhadatta et al and Maligeorgos do not disclose the receiver is characterised in that the differential quadrature low noise amplifier is constructed as a class AB operating circuit. Sano et al disclose a differential amplifier constructed as a class AB operating circuit (col 11, line 49 – col 12, line 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the amplifier as a class AB operating circuit in order to set a bis current to flow at no input signal as suggested by Sano et al (col 12, lines 7-9).

Regarding claim 13, Vishakhadatta et al and Maligeorgos disclose the method of claim 12, wherein Vishakhadatta et al and Maligeorgos do not disclose the receiver is characterised in that the differential quadrature low noise amplifier is constructed as a class AB operating circuit. Sano et al disclose a differential amplifier is constructed as a class AB operating circuit (col 11, line 49 – col 12, line 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the amplifier of Vishakhadatta et al and Maligeorgos a class AB operating circuit in order to set a bis current to flow at no input signal as suggested by Sano et al (col 12, lines 7-9).

5. Claims 5, 7, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vishakhadatta et al (US 2002/0,141,511) in view of Franca-Neto (US 6,509,799).

Regarding claim 5, Vishakhadatta et al disclose the high frequency receiver according to claim 3, wherein Vishakhadatta et al do not disclose the quadrature low noise amplifier comprises a cascode arrangement of semiconductors (20, 22). Franca-Neto discloses a low noise amplifier comprising a cascode arrangement of semiconductors (fig. 2; col 4, lines 14-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the quadrature low noise amplifier comprise a cascode arrangement of semiconductors in order to construct the amplifier into a tunable integrated circuit.

Regarding claim 7, Vishakhadatta et al disclose a front end for a high frequency receiver (839, 851), which front end comprises a low noise amplifier (LNA circuitry 824), characterized in that the low noise amplifier (LNA circuitry 824) is a quadrature low noise amplifier (LNA circuitry with in phase and quadrature outputs; para. 79; fig. 8),

characterised in that across the cascode arrangement of semiconductors there is connected a capacitor (52; fig. 2) wherein Vishakhadatta et al do not disclose the quadrature low noise amplifier comprises a cascode arrangement of semiconductors (20, 22). Franca-Neto discloses a low noise amplifier comprising a cascode arrangement of semiconductors (fig. 2; col 4, lines 14-37) and in that across the cascode arrangement of semiconductors there is connected a capacitor (52; fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect a capacitor with a cascade arrangement of semiconductors in order to tune a resonant tank circuit as suggested by Franca-Neto.

Regarding claim 14, Vishakhadatta et al disclose the method according to claim 12, wherein Vishakhadatta et al do not disclose the quadrature low noise amplifier comprises a cascode arrangement of semiconductors (20, 22). Franca-Neto discloses a low noise amplifier comprising a cascode arrangement of semiconductors (fig. 2; col 4, lines 14-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the quadrature low noise amplifier comprise a cascode arrangement of semiconductors in order to construct the amplifier into a tunable integrated circuit.

6. Claims 6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vishakhadatta et al (US 2002/0,141,511) in view of Franca-Neto (US 6,509,799) and further in view of Saigo et al (JP 57,073,974).

Regarding claim 6, Vishakhadatta et al and Franca-Neto disclose the high frequency receiver according to claim 5, wherein Franca-Neto discloses the semiconductors (transistors 20, 22) are of BJT or of a different type (col 7, lines 10-16). Vishakhadatta et al and Franca-Neto do not disclose specifically the semiconductors are MOST type. Saigo et al disclose MOST type transistors (abstract, no translation is available at this time). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have MOST type semiconductors in order to suppress variation in the threshold voltage as suggested by Saigo et al.

Regarding claim 15, Vishakhadatta et al and Franca-Neto disclose the method according to claim 14, wherein Franca-Neto discloses the semiconductors (transistors 20, 22) are of BJT or of a different type (col 7, lines 10-16). Vishakhadatta et al and Franca-Neto do not disclose specifically the semiconductors are MOST type. Saigo et al disclose MOST type transistors (abstract, no translation is available at this time). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have MOST type semiconductors in order to suppress variation in the threshold voltage as suggested by Saigo et al.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vishakhadatta et al (US 2002/0,141,511) in view of Glas et al (US 6,546,237) and further in view of Nash (US 6,317,589).

Regarding claim 8, Vishakhadatta et al disclose a high frequency receiver (839, 851), which front end comprises a low noise amplifier (LNA circuitry 824), characterized in that the low noise amplifier (LNA circuitry 824) is a quadrature low noise amplifier

(LNA circuitry with in phase and quadrature outputs; para. 79; fig. 8), which is provided with a front end comprising a low noise amplifier (LNA circuitry 824), and which is provided with quadrature mixers (dowconverting circuitry comprising I and Q mixers producing I and Q outputs) coupled to the low noise amplifier (2), characterized in that the low noise amplifier is a quadrature low noise amplifier (LNA circuitry with in phase and quadrature outputs; para. 79; fig. 8). Vishakhadatta et al do not disclose the high frequency receiver comprises two quadrature choppers coupled between respective outputs of the quadrature low noise amplifiers and respective inputs of the quadrature mixers. Glas et al disclose the high frequency receiver comprises two quadrature choppers (201, 202) and respective inputs of the quadrature mixers (208, 209) (col 2, line 63 - col 3, line 24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have choppers coupled to respective inputs of mixers in order to avoid the need for the use of analog to digital converters as suggested by Glas et al. Vishakhadatta et al and Glas et al do not disclose the choppers are coupled between respective outputs of the quadrature amplifiers and the output of mixers (110, 108) is demodulated by a quadrature demodulator. However, it is notoriously old and well known in the art to have amplifiers connected to the choppers of Glas et al in order to strengthen the received RF signal before limiting the signal. Nash discloses the output of mixers (110, 108) is demodulated by a quadrature demodulator (not shown) (col 4, lines 2-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the quadrature

demodulator of Nash to Vishakhadatta et al in order to detect the digital outputs from the mixers in a complex domain as suggested by Nash.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vishakhadatta et al (US 2002/0,141,511) in view of Glas et al (US 6,546,237) and further in view of Gratian (US 2,730,699).

Regarding claim 9, Vishakhadatta et al disclose the high frequency receiver according to claim 8, wherein Vishakhadatta et al and Glas et al do not disclose the quadrature choppers and quadrature mixers are combined to passive quadrature choppers/mixers. Gratian discloses a receiver wherein the quadrature choppers and quadrature mixers are combined to passive quadrature choppers/mixers (col 7, lines 29-31). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the limiters and mixers in order to clip the highest and the lowest amplitude while at the same time mixing the signals to a lower frequency to save circuit components.

Response to Arguments

10. Applicant's arguments filed 3/9/06 have been fully considered but they are not persuasive.

Regarding claims 3, 11, and 12, in response to applicant's argument that applicant argues that the combined cited reference, does not teach the differential amplifier, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed

invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). I and Q signals are known to be implemented differentially as is notoriously old in the art to reduce interference and noise in its output by outputting only based on a potential difference between its input terminals. The reference to the "polyphase filter" is irrelevant since as long as the LNA circuit produce the "in phase and quadrature outputs", it is not claimed that the LNA circuit cannot have a filter attached to it.

Regarding dependent claims 4-6 and 13-15, the combined references disclose the quadrature paths are implemented differentially for the reason as discussed above as in independent claim 3.

Regarding claim 7, the term "across" is discussed in the previous office action, filed 12/09/05 in the response to arguments to be broad in terms of where the capacitor is arranged with respect to the cascade arrangement.

11. Applicant's arguments with respect to claims 8-9 have been considered but are moot in view of the new ground(s) of rejection in view of the new amendment.

Also, with respect to applicant's arguments that it is "incorrect" to refer to the claimed "choppers" as "limiters", it is not defined in the specification nor the claims what "choppers" are and function to do. Therefore, the examiner's interpretation of the claimed features reads on the claimed language of a "chopper". The "high frequency receiver" as claimed is merely a receiver which is inherently capable of receiving frequencies in the wide frequency spectrum. Therefore, the combined reference

inherently teach a "high frequency receiver". The "notoriously old" statement for the combination of the limiter to limit the amplified signal, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). The combined limiter to the amplified quadrature signals of Vishakhadatta is obvious to one of ordinary skill in the art, as is also suggested in another cited reference, Maeda, where a quadrature signal is amplified and limited in an integrated unit (fig. 12; col 1, lines 55-58).

Allowable Subject Matter

11. Claims 22-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 22, Vishakhadatta et al and Glas disclose the receiver of claim 8, wherein Vishakhadatta et al, Glas and the cited prior art fail to disclose each of said choppers switches its respective outputs for coupling with the other of said choppers.

Regarding claim 23, Vishakhadatta et al and Glas disclose the receiver of claim 8, wherein Vishakhadatta et al, Glas and the cited prior art fail to disclose said choppers switch in-phase and quadrature signals.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N Le whose telephone number is (703) 308-5836. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F Urban can be reached on (703) 305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lana Le

Lana N Le
5-24-06

LANA LE
PRIMARY EXAMINER